09/281,973

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     FILE 'USPATFULL' ENTERED AT 20:14:08 ON 30 AUG 2001
L1            24 S FIRST PIN# (P) FIRST SIGNAL#
L2            25 S SECOND PIN# (P) SECOND SIGNAL#
L3           718 S TEST SIGNAL GENERATING CIRCUIT# OR TEST SIGNAL GENERATOR#
L4         10841 S TEST SIGNAL#
L5           718 S L3 (P) L4
L6           163 S LOGICAL COMBINATION AND (FIRST SIGNAL# (P) SECOND SIGNAL#)
L7            16 S L1 (P) L2
L8          2301 S LOGICAL COMBINATION OR COMBINATION LOGIC
L9           163 S L6 AND L8
L10       533892 S PIN#
L11           75 S L10 AND L9
L12            3 S L11 AND L4
                 SAVE PHUNG/L ALL

=> d l12 ibib ti 1-3


L12  ANSWER 1 OF 3  USPATFULL
ACCESSION NUMBER:        2000:85667  USPATFULL
TITLE:                   Data processing devices, systems and methods with mode
                         driven stops
INVENTOR(S):             Swoboda, Gary L., Sugar Land, TX, United States
                         Daniels, Martin D., Houston, TX, United States
PATENT ASSIGNEE(S):      Texas Instruments Incorporated, Dallas, TX, United
                         States (U.S. corporation)

                              NUMBER        KIND    DATE
                         ---------------- ------ --------
PATENT INFORMATION:      US 6085336              20000704
APPLICATION INFO.:       US 1992-827549          19920129  (7)
RELATED APPLN. INFO.:    Continuation of Ser. No. US 1989-387475, filed on 31
                         Jul 1989, now abandoned which is a
continuation-in-part
                         of Ser. No. US 1987-57078, filed on 2 Jun 1987, now
                         patented, Pat. No. US 4860290 And Ser. No. US
                         1987-93463, filed on 4 Sep 1987, now abandoned
DOCUMENT TYPE:           Utility
FILE SEGMENT:            Granted
PRIMARY EXAMINER:        Treat, William M.
LEGAL REPRESENTATIVE:    Marshall, Jr., Robert D., Donaldson, Richard L.
NUMBER OF CLAIMS:        32
EXEMPLARY CLAIM:         1
NUMBER OF DRAWINGS:      46 Drawing Figure(s); 53 Drawing Page(s)
LINE COUNT:              4161
TI     Data processing devices, systems and methods with mode driven stops

L12  ANSWER 2 OF 3  USPATFULL
ACCESSION NUMBER:        1999:31667  USPATFULL
TITLE:                   Memory system having non-volatile data storage
                         structure for memory control parameters and method
INVENTOR(S):             Roohparvar, Frankie F., Cupertino, CA, United States
PATENT ASSIGNEE(S):      Micron Technology, Inc., Santa Clara, CA, United
States
                         (U.S. corporation)

                              NUMBER        KIND    DATE
                         ---------------- ------ --------
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PATENT INFORMATION: US 5880996 19990309
APPLICATION INFO.: US 1997-850582 1997[illegible]2 (8)
RELATED APPLN. INFO.: Continuation of Ser. No. US 1995-508923, filed on 28 Jul 1995, now patented, Pat. No. US 5627784
DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Nguyen, Viet Q.
LEGAL REPRESENTATIVE: Schwegman, Lundberg, Woessner & Kluth, P.A.
NUMBER OF CLAIMS: 30
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 20 Drawing Figure(s); 19 Drawing Page(s)
LINE COUNT: 1948
TI Memory system having non-volatile data storage structure for memory control parameters and method

L12 ANSWER 3 OF 3 USPATFULL
ACCESSION NUMBER: 75:15536 USPATFULL
TITLE: ELECTRONIC TESTER FOR TESTING DEVICES HAVING A HIGH CIRCUIT DENSITY
INVENTOR(S): Barnard, John Dudley, Wappingers Falls, NY, United States
PATENT ASSIGNEE(S): International Business Machines Corporation, Armonk, NY, United States (U.S. corporation)

	NUMBER	KIND	DATE	
PATENT INFORMATION:	US 3873818		19750325	
APPLICATION INFO.:	US 1973-410592		19731029	(5)

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Gruber, Felix D.
ASSISTANT EXAMINER: Dildine, Jr., R. Stephen
LEGAL REPRESENTATIVE: DeBruin, Wesley
NUMBER OF CLAIMS: 51
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 11 Drawing Figure(s); 7 Drawing Page(s)
LINE COUNT: 3016
TI ELECTRONIC TESTER FOR TESTING DEVICES HAVING A HIGH CIRCUIT DENSITY

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> d l12 kwic 1-3

L12  ANSWER 1 OF 3  USPATFULL
DRWD    FIG. 36 is a pictorial of an improved pin-out or bond-out
        configuration for a chip carrier for the data processing device of
FIGS.
        1A and 1B illustrating improvements applicable.  .  .
DRWD    FIG. 40 is a version of the improved pin-out configuration in
        a single in-line type of chip;
DRWD    FIG. 41 is another version of the improved pin-out
        configuration;
DRWD    FIG. 42 is a pictorial of a dual in-line construction wherein the
        improved pin-out configuration is applicable and showing
        translation arrows;
DRWD    FIG. 43 is a pictorial of some pins of a pin grid
        array construction wherein the improved pin-out configuration
        is applicable;
DETD    .  .  .  full-speed execution and monitoring of each target chip such
as
        device 11 in the user's target system 1043 via a multi-pin
        target connector. In one embodiment, thirty software and hardware
        breakpoints, software and hardware trace and timing, and single-step
        execution are.  .  .
DETD    Full-speed execution and monitoring of the target system is suitably
        controlled via a multi-wire interface or scan path in the multi-
      pin target connector. The scan path controls the target chip in
        the system 1043, providing access to all the registers as.  .  .
DETD                     .  .  .  Clock
              No         Yes        Yes
Independence
Boundary Scan Support
              No         Yes        Yes
Silicon Efficiency
              Yes        No         Yes
Most Emulation Capability
              No         Yes        Yes
Number of Extra Pins
              Four       Six        Six
_______________________________________
DETD    .  .  .  improved SCOPE hardware which is provided on each of the chips
        such as device 11 on PC board 1043. Four pins TDI, TMS, TCK
        and TDO communicate with the system. TMS and TCK communicate with a tap
        controller 1151 which is.  .  .
DETD    Generally, in FIG. 50, serial information is down loaded from emulation
        computer 1101 via the SCOPE controller card 1141 through pin
        TDI and enters any one of a number of shift registers, including a
        boundary scan register 1161, a device identification.  .  .  send
serial
        outputs from all parts of the on-chip JTAG circuitry back to computer
        JTAG card 1141 via output serial pin TDO.
DETD    In a previous approach, a cable is terminated in a pin-plug
        that mates to a socket provided on the board in place of the emulated
        device. The socket introduces a noise.  .  .
DETD    The few pins utilized by the scan interface 1150 eliminate the
        need for conventional full pin-out target connectors and
        eliminate problems associated with cable reliability, transmission
        effects and timing differences. In this way, board 1043 can.  .  .
DETD    .  .  .  more of the selected areas of boundary scan area 1211 which
```

DUT **pin**, applies the load to the DUT **pin**, and masks the rendition of the GO/NO GO manifestation.

DETD . . . from FIG. 10 that AND circuit 11 will be energized at y-time, where a logical one is impressed on the **pin** circuit input. The output of Latch 24 will rise to the UP level at y-time when a d bit is. . .

DETD When a logical one is impressed on the input of the **pin** circuit, the clock inputs of Latches 22,23 and 24 will be conditioned at y-time, via AND circuit 11. AND circuit. . .

DETD . . . Latch 35 (FIG. 6) at y-Time. In the presence of a logical one of test data being impressed on the **PIN** circuit input from the Shift Register Means, the output of Latch 35 will rise to the UP level. The UP. . .

DETD The Operational Code 1001,SET **PIN** SERIAL (SPS)

DETD . . . 6) at y-time. In the presence of a logical one of test data being impressed on the input to the **pin** circuit the output of Latch 21 will rise to the UP level at y-time. The UP output of Latch 21,. . .

DETD When the Operational code calls for SET DISCONNECT, namely the **logical combination** abcd for clock input of Latch 20 (FIG. 6) is set at y-time. When the data input to the **PIN** CIRCUIT is a logical one, the output of Latch 20 will rise to the UP level. The UP output of. . . When a DOWN input is impressed on the control input of Switch 34 the Switch opens, and thereby disconnects the **pin** of the device under test from the **PIN** Electronic circuit.

DETD . . . The Test Tester command, via OR circuit 27 (FIG. 6), conditions the upper input of AND circuit 31 of the **Pin** circuit (FIG. 6). The Test mode electrical manifestation from AND circuit 85 is impressed on and conditions the lower input. . . Latch 26 and provides an electrical manifestation, namely a logical one, or UP level, on the GO/NO-GO line of the **Pin** circuit.

DETD . . . sets a logical one in Latch 23. With the output of Latch 23 UP the following conditions exist in the **Pin** circuit of FIG. 6; switch 33 is closed; the lower input of AND circuit 28 is conditioned; and the center. . .

DETD Now further assume for purposes of explanation that the test bit impressed on the input to the **PIN** circuit during the TEST PARALLEL operation is a logical zero. Thus a DOWN level electrical manifestation is impressed on the. . .

DETD . . . at Drive-Time the output of Latch 25 will be at a Down level, manifesting that the test bit for the **Pin** circuit was a logical zero. The DOWN output of Latch 25 is coupled via Exclusive OR circuit 37 to the. . . output of Latch 25 the Driver 29 impresses, or drives, an electrical manifestation representative of a logical zero on the **pin** of the device under test. Namely, as represented in FIG. 6 the potential V.sub.2 is impressed via switches 33 and 34 on the **Pin** of the Device under Test. Note, if the test bit had been a logical one an electrical manifestation of a logical one would have been impressed on the **pin** of the device under test. In FIG. 6 the potential V.sub.1 is represented as the electrical manifestation of a logical one impressed on the **pin** of the device under test.

DETD . . . have the magnitudes of V.sub.1 and V.sub.2 respectively set by the controller, or they may be respectively set at the **pin** circuits.

DETD Now assume that prior to the current TEST SERIAL operation a SET **PIN** SERIAL operation has been executed by the tester. The SET **PIN** SERIAL operation will have set Latch 21 in any predetermined one of the n **Pin** circuits. Namely, the **Pin** circuit that is sto receive a series of test bits (one per test step) during a

TEST SERIAL operation. There. . . .

DETD Assume merely for purposes of explanation that Latch 21 of **PIN** CIRCUIT PEN, shown in FIG. 6, has a logical one stored therein by an earlier SET **PIN** SERIAL operation. As explained earlier, during an SPS operation Latch 21 is set by a logical one being impressed on the **pin** circuit input in the presence of the SPS command, (abcd) at y-time. The UP output of the Latch 21 via. . . .

DETD Thus at the initiation of the current TEST SERIAL operation the **pin** circuits have been set. Namely, only **PIN** circuit PEN shown in FIG. 6 will respond to, or accept a test data input. (Note, only **PIN** circuit PEN has Latch 21 set.)

DETD The following conditions exist in **PIN** circuit PEN at the initiation of TEST SERIAL: Latch 21 is set; Latch 23 is set; AND circuit 28 is. . . .

DETD . . . 3, 5, 7----95, 97 and 99, Driver 29 will drive an electrical manifestation of a logical one on the n.sup.th **pin** of the device under test. Namely during each odd numbered test step the data input of Latch 25 has a. . . .

DETD . . . level input from Latch 25 will drive a logical one electrical manifestation via closed switches 33 and 34 to the **pin** of the device under test. Namely, in this example, the **pin** of the device under test which is connected to **PIN** circuit PEN.

DETD . . . to an UP level, impresses a first electrical condition or manifestation, in the instant case a potential, on the n.sup.th **pin** of the device under test. The Driver 29, in response to a DOWN level, impresses a second electrical condition or manifestation, in the instant case, a potential on the n.sup.th **pin** of the device under test.

DETD Now referring to FIG. 6, consider the case where the **PIN** circuit is connected to an output **PIN** of the device under test. Assume further that the output **PIN** of the device under test requires a load to be applied thereto. The operational code SET-LOAD, OUT, MASK (0100) SLIM. . . . 22 set, switch 32 will be closed. Thus the load is applied via switches 32 and 34 to the output **pin** of the device under test.

DETD In FIG. 6 the input of Detector 30 is connected via junction J.sub.1, through switch 34 to the output **pin** of the device under test. During a test step, which may be a test step under a TEST SERIAL, or TEST PARALLEL operation, the output of the device under test electrically manifested at the output **pin** connected to switch 34 of FIG. 6 will be impressed on the input of Detector 30. Detector 30 will provide. . . .

DETD . . . AND circuit 14, at STROBE-Time. Thus, the output of Latch 26 will be UP when the output from the output **pin** of the device under test is equal to, or greater than V.sub.3 and the test data input to Exclusive OR 13 is a logical zero. The output of Latch 26 will be DOWN when the output from the output **pin** of the device under test is less than V.sub.3 and the test data input to Exclusive OR 13 is a. . . .

DETD All n **pin** circuits in the disclosed embodiment are stated and represented to be identical. It will be appreciated that such is not a requirement for the practice of applicant's invention. Applicant's invention may be practiced with n **pin** circuits varying one from the other in function, or logical content, or technology employed. The **pin** circuits must meet the needs of the tester as dictated by the objective to effectively and efficiently test the device. . . .

DETD The GO/NO-GO signals provided by the **pin** circuits are preferably conveyed to the Controller for storage, analysis and/or processing. They may be conveyed on a per **pin**, per test step basis, or any manner that aids in the efficient effective testing of the

device under test. The GO/NO-GO signals from a number of **pin** circuits, or all **pin** circuits connected to output **pins** of the device under test, may be ORred together and a single GO/NO-GO signal sent to the Controller.

DETD . . . W.sub.fl further illustrates the impressing of the associated operational code specifying bits, as explained earlier herein, on the Decoder and **PIN** circuits for essentially the full duration of each test step.

DETD . . . (SD) electrical manifestation occurring only during a test cycle employed to execute the operational code SET Disconnect (SD); a SET **PIN** SERIAL (SPS) electrical manifestation occurring only during a test cycle employed to execute the operational code SET **PIN** SERIAL; or a SET Clock 1 (SC1) electrical manifestation occurring only during a test cycle employed to execute the operational. . . .

CLM What is claimed is:

1. An electronic test system for testing high density logic networks, said networks having n contact **pins**, each of said contact **pins** having associated therewith a function, where n is an integer having any value in the range of one hundred through. . . for specifying an operational code for each word of test data stored in said word oriented random access memory; n **pin** circuits each having at least a test data input, and an output, each of said **pin** circuits being settable to perform any one of a plurality of functions, each of said n outputs of said n **pin** circuits being connected to a discrete one of said n contact **pins** of a network under test; a closed loop high speed shift register having n stages, each stage of said shift. . . random access memory, and an output coupled to a predetermined one of said n test data inputs of said n **pin** circuits; decode circuitry intercoupling said system controller, said operational code specifying means, said shift register and each of said n **pin** circuits, said decode circuitry being adapted to, during each test step, in response to an input from said operational code specifying means, and under control of said system controller, selectively control at least each of said n **pin** circuits and said shift register, whereby during each of said m test steps an n bit binary word is impressed on said n contact **pins** of a network under test, and whereby said word oriented random access memory contains in said z word storage positions. . .

. . . one timing signal from said system controller, said circuit means including means for electrically manifesting to each of said n **pin** circuits and said shift register at least certain operations called for by said operational code specifying binary bits.

. . . there is a discrete operational code for at least one of the following opertion: SET NUMBER OF SERIAL TESTS; SET **PIN** SERIAL; TEST SERIAL; TEST PARALLEL; TEST TESTER; SET CLOCK 1; SET DISCONNECT; SET-LOAD, OUT, MASK; SET-LOAD, OUT, MASK; SET-LOAD, IN,. . .

. . . following operational codes are respectively specified by a discrete one of said binary words, SET number of SERIAL TESTS, SET **PIN** SERIAL, TEST SERIAL and TEST PARALLEL.

. . . said shift register; a second group of outputs of said decode circuitry interconnecting said third circuit means and said n **pin** circuits, whereby each of said n **pin** circuits and said shift register function in accordance with the operational codes called for by the operational code specifying bits.

. . .

. . . one thousand, said method employing test apparatus including test system controller means, word oriented random access storage means, n discrete **pin** circuit means coupled to n **pins** of a

device under test, and binary word assembly means, said method comprising the steps of: a. conditioning each of said n **pin** circuit means to perform a discrete one of a plurality of functions, where said functions include input, output, driver, load,. . . and said functions are in accordance with the function of the terminal of the device under test to which the **pin** circuit is coupled. b. obtaining during a first test step a first one of said m discrete n binary bit. . . test words from said word oriented random access storage means, c. impressing said first test word on said n discrete **pin** circuit means, d. obtaining during a second test step a predetermined portion of a second one of said m discrete. . . word and said predetermined portion of said second test word, f. impressing said second test word on said n discrete **pin** circuit means.

. . . wherein during each of said m steps a discrete n binary bit test word is impressed on said n discrete **pin** circuit means, and during at least certain of said test steps a determination is made as to the merit, or. . .

14. In a test method as recited in claim 13 wherein each of said n **pin** circuits means is settable to perform one of the afore-identified functions, a plurality of said **pin** circuit means set to perform an output function, at least one of said plurality of output **pin** circuit means being adapted to receive an electrical manifestation varying in time in an anticipated prescribed manner from said device. . .

. . . said m test steps where said test apparatus is operating in the Set-UP MODE at least certain of said n **Pin** circuit means are set-up to perform a predetermined function.

20. An electronic tester for testing large scale integration devices, said devices having n contact **pins**, where n is an integer having a magnitude of at least one hundred, said tester being under control of a. . . bits, said shift register means being adapted to successively receive n binary bits of test data from said memory; n **pin** circuits means coupled to said controllable shift register means and said n contact **pins** of a device under test; control means for controlling said shift register means and each of said n **pin** circuit means, said control means interconnecting said shift register means and said n **pin** circuit means, said control means cooperating with said computer system and being successively responsive to binary values obtained from said. . .

. . . by said test system for the associated n binary bits of test data, where z is an integer; n settable **pin** circuits each having a data input and an output, each of said n **pin** circuits including settable means for setting the function of said **pin** circuit; connection means connecting each of said n outputs of said n **pin** circuits to a discrete one of said n contact pads of said device under test; high speed recirculating shift register. . . connecting said n outputs of said n stages of said shift register means and said n inputs of said n **pin** circuit means; decode circuit means intercoupling said system controller, said word oriented random access memory, said shift register means, auxiliary means and said n **pin** circuit means, specifying bits from said word oriented random access memory and to cause said test system to execute the. . .

. . . 30. An electronic test system as recited in claim 23 further characterized by at least one of said n settable **pin** circuits being a **pin** circuit for use in a high speed tester for testing large scale integration devices, where said tester employs at least a plurality of operational code specifying bits, a SET DISCONNECT electrical manifestation, a TEST PARALLEL electrical manifestation, a SET **PIN** SERIAL electrical manifestation, a TEST TESTER electrical manifestation, a SET-UP mode electrical instruction, a SET CLOCK 1 electrical manifestation, a. . . mode electrical instruction,

DRIVE TIME pulses, STROBE TIME pulses and CLOCK 1 pulses and provides at least GO/NO-GO pulses, said **pin** circuits being conditionable to perform a plurality of functions expressly including the following, driver, load, open and ground, said **pin** circuit comprising: a test data input terminal for accepting test data and a DUT connection terminal for connection to a contact **pin**, or pad, of a large Scale integration device under test; first, second, third, fourth, fifth, sixth, seventh and eighth settable. . . settable DETECTOR circuit having an input and an output, said DETECTOR circuit being adapted to provide as an output a **first signal** when an electrical status equal or to or less than a predetermined set standard is impressed on the input thereof and a **second signal** when an electrical status greater than said predetermined set standard is impressed on the input thereof; an electrical load; first connection means connecting in common said data input terminal of said **pin** circuit, said information input of said first latch, said information input of said second latch, said second input of said. . . switch; fourth connection means connecting said second terminal means of said first switch and said DUT connection terminal of said **PIN** circuit; fifth connection means connecting said second terminal means of said second switch to said electrical load; said first input. . . to receive a TEST PARALLEL electrical command, said control input of said second latch being adapted to receive a SET **PIN** SERIAL electrical command, said second input of said first OR circuit being connected to said output of said second latch,. . . output of said seventh AND circuit being connected to said first input of said second Exclusive OR circuit; whereby said **pin** circuit is conditionable to perform any one of said plurality of functions respectively in accord with the operation of said. . .

. . . 23 wherein said operational code specifying bits during at least one of said m test steps specifies the operation SET **PIN** SERIAL and in response thereto said test system executes the operation SET **PIN** SERIAL.

. . . following SET NUMBER SERIAL TESTS command, TEST SERIAL command, NOT TEST SERIAL command, TEST MODE command, SET DISCONNECT command, SET **PIN** SERIAL command, TEST PARALLEL command, TEST TESTER command, a SETUP MODE command, a SET CLOCK 1 command, a STOP RAM. . . input terminal of said Decode circuit, and said output of said fifth AND circuit being adapted to provide a SET **PIN** SERIAL command; said second input of said sixth AND circuit being connected to said third input terminal of said Decode. . . execute upon command a SET SERIAL NUMBER of TESTS operation, a TEST SERIAL operation, a SET DISCONNECT operation, a SET **PIN** SERIAL operation, a TEST PARALLEL operation, or a TEST TESTER operation.

49. A **pin** circuit for use in a high speed tester for testing large scale integration devices, where said tester employs at least a plurality of operational code specifying bits, a SET DISCONNECT electrical manifestation, a TEST PARALLEL electrical manifestation, a SET **PIN** SERIAL electrical manifestation, a TEST TESTER electrical manifestation, a SET-UP mode electrical instruction, a SET CLOCK 1 electrical manifestation, a. . . mode electrical instruction,

DRIVE TIME pulses, STROBE TIME pulses and CLOCK 1 pulses and provides at least GO/NO-GO pulses, said **pin** circuit being conditionable to perform a plurality of functions expressly including the following, driver, load, open and ground, said **pin** circuit comprising: a test data input terminal for accepting test data and a DUT connection terminal for connection to a contact **pin**, or pad, of a large scale integration device under test; first, second, third, fourth, fifth, sixth, seventh and eighth settable. . . settable DETECTOR

circuit having an input and an output, said DETECTOR circuit being adapted to provide as an output a **first signal** when an electrical status equal to or less than a predetermined set standard is impressed on the input thereof and a **second signal** when an electrical status greater than said predetermined set standard is impressed on the input thereof; an electrical load,; first connection means connecting in common said data input terminal of said **pin** circuit, said information input of said first latch, said information input of said second latch, said second input of said. . . switch; fourth connection means connecting said second terminal means of said first switch and said DUT connection terminal of said **PIN** circuit; fifth connection means connecting said second terminal means of said second switch to said electrical load; said first input. . . to receive a TEST PARALLEL electrical command, said control input of said second latch being adapted to receive a SET **PIN** SERIAL electrical command, said second input of said first OR circuit being connected to said output of said second latch,. . . output of said seventh AND circuit being connected to said first input of said second Exclusive OR circuit; whereby said **pin** circuit is conditionable to perform any one of said plurality of functions respectively in accord with the operation of said. . .

. . . following SET NUMBER SERIAL TESTS command, TEST SERIAL command, NOT TEST SERIAL command, TEST MODE command, SET DISCONNECT command, SET **PIN** SERIAL command, TEST PARALLEL command, TEST TESTER command, a SET-UP MODE command, a SET CLOCK 1 command, a STOP RAM. . . input terminal of said Decode circuit, and said output of said fifth AND circuit being adapted to provide a SET **PIN** SERIAL command; said second input of said sixth AND circuit being connected to said third input terminal of said Decode. . . execute upon command a SET SERIAL NUMBER of TESTS operation, a TEST SERIAL operation, a SET DISCONNECT operation, a SET **PIN** SERIAL operation, a TEST PARALLEL operation, or a TEST TESTER operation.

includes BSR 1161 of FIG. 50 and scans the **pin** boundary of device 11. The FIG. 51 domains--CPU core domain 1213, system domain 1215 and analysis domain 1217 are shown. . . .

DETD . . . shows a physical perspective of the various domains on the chip of device 11. JTAG control 1201 interfaces with the **pins** via a serial boundary scan assembly including boundary scan register 1161 which allows all logic states at the actual **pins** of device 11 to be read or written. JTAG TAP controller 1151 and JTAG instruction register IR 1153 are provided. . . . control 1203 serially interfaces with the domains for core 1213, system 1215 and analysis 1217 for the device 11. Bi-directional **pins** EMU0 and EMU1 are provided for external interfacing in addition to the four JTAG terminals 1221. Combining JTAG testability interface technology with MPSD modular port scan with the additional **pins** EMU0 and EMU1 synergistically opens up capabilities for integrating emulation, software development, and manufacturing and field test processes.

DETD . . . control 1203 allow independent selection of functional clock FCLK (chip clock rate divided by two) or scan clock JCLK (TCK **pin** of FIG. 50). Each domain 1213, 1215, 1217 can have its clock individually selected while other domain selections are locked. . . .

DETD . . . signal that indicates the core is running, so that just when the core ceases running, the DONE signal is provided. **Pins** EMUL and EMU0 carry signals of same designation originating internally or externally of the chip for emulation signaling.

DETD . . . connected to an input of the combining circuit 1705 for supplying ANASTP, but also is connected directly to an output **pin** EMU0.

DETD In another filter example, the counter borrow line is selected by scan register 1711.1 and fed out of **pin** EMU0 to permit external logic to count events at a rate stepped down by frequency division by the value in. . . .

DETD . . . can be provided by the skilled worker according to the principles set forth herein to provide sensor logic for any **logical combination** of conditions so that occurrences of any complex combination of conditions or sequence of conditions can be sensed. The breakpoint. . . .

DETD . . . which is to be provided later. Device 11 includes an electronic processor CPU 1873 which is operable to generate a **first signal** to access the peripheral 1871. Peripheral 1871, if it were present, would reply with a **second signal** on a line ME 1875 if the access is either a Read or a Write. When the access is a. . . .

DETD A sensing circuit 1877 is connected to the electronic processor 1873 to temporarily suspend operations of CPU 1873 when the **first signal** is sent by CPU 1873 in an attempt to access the peripheral 1871. sensing circuit 1877 is interconnected with analysis. . . . host computer 1101 via the scan path earlier described. Host computer 1101 simulates the absent peripheral 1871 and determines what **second signal** the peripheral 1871 would supply. Then in simulation of that peripheral 1871, host computer 1101 down loads a serial bit stream along line 1103 into interface 1881. Thereupon the interface 1881 supplies the **second signal** which peripheral 1871 would have supplied in response to the CPU 1873. In this way, CPU 1873 receives a signal. . . .

DETD . . . has a first circuit but lacks a second circuit which is to be provided later. The first circuit sends a **first signal** to which a second circuit when present would reply with a **second signal**.

DETD In FIG. 77 the method commences with a START 1901 and proceeds to a step 1903 to sense the **first signal** sent by the first

circuit to access the second circuit. Then in a step 1905, the process temporarily suspends operation by the first circuit when the **first signal** is sensed. Next, a step 1907 simulates the second circuit to generate a representation of the **second signal**. A subsequent step 1909 loads the representation of a **second signal** into an interface to the first circuit. Final step 1911 resumes operation of the first circuit so that the first circuit receives the **second signal** as a simulated reply from the interface. Upon completion of step 1911, operations return to start 1901 to repeat the. . .

DETD . . . clock JCLK, and enables simulation of peripheral functions. The interface further provides extensive internal testing for complex devices in low **pin**-count packages. The flexible circuitry of the interface used with host computer 1101 reduces device prototype to production time, and improves. . . boundary scan capability is particularly important as board densities increase and the use of surface mount devices with less accessible **pins** increases.

DETD . . . development system polls status through the scan serial port or receives interrupts from the microcontroller via the EMU0 or EMU1 **pins** of FIG. 53.

DETD . . . 2250, instruction cache 2230, and Input/output registers 2260. Host interface 2240 and memory interface 2250 are respectively externally accessible via **pins** and buses 2115 and 2122. A video display controller 2270 associated with I/O registers 2260 supplies its output on a. . .

DETD . . . logic is included to ensure that there is a route from each of these registers to local address data (LAD) **pins** of the chip.

DETD . . . of core processing circuitry 2101 on chip. These are put on two scan paths and are accessible via two bidirectional **pins** SCIN and SCOUT- in test mode. Extra latches are suitably placed as desired to easily observe key logic elements.

DETD The GSP 2120 incorporates four-phase active-low clocks Q1N through Q4N of FIG. 82 generated from the input clock **pin**. Also present are four active-high half-phase clocks H1T through H4T. As stated previously, all memory elements are loaded only during. . .

DETD . . . to utilize the parallel and serial latches, control hardware is included and connected to reset, run/emu, local interrupt, and hold **pins**. When both reset and run/emu are pulled low, the values presented on two local interrupt **pins** and the hold **pin** provide a 3-bit code which is decoded into one of seven possible test modes.

DETD . . . 2270 has its own independent two-phase clocking scheme with internal phases V5T and V6T derived from a video input clock **pin** (VCLK). Registers 2260 used by the video controller are loaded on V6T only. To get around this in all test modes, the video clocks are disconnected from the VCLK **pin** and the two phases are "joined" to H3T and H1T. Then all the video registers are loaded on V6T, the. . .

DETD . . . connected to a selecting multiplexer MUX 2113 connected to serial data in SCIN 2115 and serial data out SCOUT- 2117 **pins**. Emulation control **pins** EC0 and EC1 provide further control inputs. All of the four wires of interface 2111 are connected via a selector. . . 2135 and core 2101. The third path connects to a MUX 2113. The selection is also controllable by emulation control **pins** EC0 and EC1, which correspond to **pins** EMU1 and EMU0 earlier described.

DETD Test modes are controlled via the EC1, EC0 and SCIN **pins**, and two bits TEST and COMPRESS of the emulation control register 2121.

DETD The control **pins** EC1, EC0 and SCIN initially define the state

of the emulation control port. Scanning a 1 into the TEST bit. . . .

DETD One major advantage of this type of test is that it can be performed with a simple, low-performance, low-**pin** count tester, but gives excellent fault coverage.

DETD For parallel load and dump PLOAD and PDUMP, start and execute states are generated internally. Externally, the **pins** are timed with a set up time of 20 nanoseconds and a zero hold time with respect to rising transition. . . .

DETD SCOUT- is an output **pin** that is used for scan output of data in the scan mode and for output of a stop acknowledge indication. . . .

DETD . . . emulation hardware sets a halt code on EC1, EC0, and SCIN and awaits a stop acknowledge STOPACK on the output **pin** SCOUT-.

DETD The codes available at the **pins** EC1, EC0 and SCIN are as follows: Normal functional mode, controlled execution mode, halt, pause, emulation control register scan and. . . .

DETD The normal functional mode is utilized in design of systems and is obtainable by letting the emulation **pins** float electrically. The **pins** have a pull up resistor on chip. The normal functional mode disables the internal control registers 2103, 2105 and 2107. . . .

DETD . . . bit). Emulator control register 2121 is scannable in response to the Table VI code "emulation control register scan" applied to **pins** EC1 and EC0.

DETD 1. A halt code on the emulation **pins**;

DETD . . . and a software trap is taken in executing the microcode when a stop condition is required. If the emulation control **pins** are in any other state, the presence of an emulator or host computer 1101 is assumed and the CPU 2101. . . .

DETD . . . functions except the software trap. Instead of the software trap, the CPU waits for a HALT code on the emulator **pins** and then lastly enters halt microcode. Where CPU 2101 is part of a graphics signal processing chip (GSP), the memory. . . .

DETD TABLE VII

	Parameter	Min	Max	Unit
Tsu(EC-CLK1H)	Setup time of EC **pins** valid before CLK1 high	20		ns
Thd(EC-CLK1K)	Hold time of EC **pins** valid after CLK1 high	0		ns
Td(CLK1H-SCOUTL)	Delay time from CLK1 high to SCOUT low		20	ns
Td(CLK1K-SCOUTH)	Delay time from CLK1		20	ns

. . .

DETD . . . CPU to execute one instruction

17	CPU priority	Raises CPU priority above Host
18	Device disable	Disables the device and tri-states all **pins**
19	EMUReset	Emulator generated reset
20	EMUINT	Forces emulator to halt during an idle instruction or pixblt
29	Cache flush flag	Indicates a. . . .

DETD . . . enable bit 10 of register 2121. Second, the emulator enters the
controlled execution mode. Third, the CPU 2101 forces SCOUT **pin** high. Fourth, the CPU 2101 places a 32 bit word of the machine state in register 2105 and forces SCOUT **pin** low. Fifth, CPU waits for the cycle to complete. When emulator busy bit is enabled, the CPU signals stop acknowledge STOPACK on the SCOUT **pin** low. Sixth, the emulator enters a data scan mode and scans the register 2105. When scanning, the CPU 2101 is. . . .

DETD . . . Write Protect features. When this bit is set, the time multiplexing on the PAGMD-, BUSER, and the Size 16 - **pin** is also enabled during normal functional mode this bit is cleared to zero.

DETD . . . register 2121 causes core 2101 to execute only one instruction before generating a stop acknowledge STOPACK signal on the SCOUT- **pin** to indicate an emulation stopped condition. This is similar to forcing an emulation instruction into the instruction stream after the. . . .

DETD . . . be interrupted. This bit is effective when both it is set and the halt code is placed on the emulator **pins**.

DETD A BUSERR flag indicates that a memory bus error has been detected on the
BUSER and LRDY **pins** during a current emulator memory access. This flag is automatically cleared when scanned out. During normal functional mode, this flag. . . .

DETD A RETRY flag 30 indicates that the target system has requested a memory retry on the BUSERR and LRDY **pins** during the current emulator memory access. This flag is automatically cleared when scanned out. During normal functional mode, this flag. . . .

DETD . . . wait in a loop until a halt code is present. When the emulator computer 1101 establishes the halt signal on **pins** EC0 and EC1, CPU 2101 jumps to emulation halt microcode.

DETD In the emulation mode, for example, the emulation hardware uses the multiplexed emulation **pin** functions to start and stop, single step, execute macro instructions, scan out and scan in internal machine status. A typical. . . .

DETD TABLE XII

Emulation **pins**	Scan Data
HALT	Set Data SCAN=MA
Wait for SCOUT- low	
	MA=0X801000
Scan EMU Control	SCAN=MD, FCN=WRITE MEM,
Scan DATA	EMU Busy En=1
Scan EMU Control. . . .	

DETD . . . for initial power up. Reset should be blocked when the halt, pause, or scan modes are placed on the emulator **pins**. Reset should also be blocked when in the MACRO mode. Further, in other than normal functional mode, the memory controller. . . .

DETD . . . was at execution start.

XO	eXecute cOnnect-functionally connects the emulator to the target system.
XR	eXecute Reset-reset TMS320C30 as if the **pin** RESET was asserted. The value at the reset vector address (0x000000) is placed in the PC.

CLM What is claimed is:
. . . with said mode register for connecting the shift register latches in a serial chain having a test input for supplying **test signals** thereto and a test output for obtaining test results therefrom, the **test signals** thereby defining the selected stop to be executed.

L12 ANSWER 2 OF 3 USPATFULL

DETD . . . 12 is to be erased (either in bulk or by block), the associated processor will cause the output enable OE **pin** to be inactive (high), and the chip enable CE and write enable WE terminals to be active (low). The processor. . .

DETD . . . state on the falling edge of output S.sub.1 thereby providing a signal with a nominal period of 6 microseconds. The **logical combination** of S.sub.1 * S.sub.2 is equivalent to subtracting 1.5 microseconds (signal S.sub.1) from 6 microseconds (signal S.sub.2) to arrive at. . .

DETD . . . which is the case. In addition, the test mode format check and decode logic 262 will produce a decode output **test signal** TM indicating that one of the three test modes associated with the data storage units has been entered. Addresses A15. . .

DETD . . . be loaded, addresses A15 and A16 are coupled to two inputs of a NAND gate 276. The remaining input is **test signal** TM which went high at time T.sub.0. Thus, the output of gate 276 will go active or low by producing. . .

DETD . . . at time T.sub.7 thereby causing the memory system to exit the test mode as indicated by the falling edge of **test signal** TM.

CLM What is claimed is:

. . . for providing an interface between the memory system and an environment external to the memory system, the terminals receive a **first signal** when the memory is in the normal operating mode and a **second signal** the memory is in the alternative test mode.

7. The memory system of claim 5 wherein the **first signal** functions as an address signal when the memory system is in the normal operating mode, and the **second signal** functions as control parameter data.

L12 ANSWER 3 OF 3 USPATFULL

SUMM . . . that an apparatus for testing LSI circuits must be able to develop and analyze a large quantity of data and **test signals**. Moreover, the test system should be operable over a wide range of signal frequencies which are commonly used in the. . .

SUMM . . . primary control over the test system and establishes the test sequence and parameters according to an operational test program. Each **pin** of the device under test has its own **pin** electronic circuit. Where the device under test has n **pins**, n **pin** electronics circuits, or cards, are required.

SUMM Binary words each having n binary bits are successively impressed on said **pin** electronics cards. Whereby each of said n **pin** electronics cards receives a logic "zero" electrical manifestion or a logic "one" electrical manifestation, as called for by the test. . . controller and decode circuitry the n bit binary words are, each during a discrete time period, applied to said n **pin** electronics circuits. Each **pin** electronics circuit includes switches interconnecting analog to digital conversion circuitry and digital to analog conversion circuitry. The switches of each **pin** electronics circuit card are controlled by said system controller and Decode circuitry to provide any one of at least the. . . following circuit functions: driver, detector, load, power supply, ground and open circuit. Thus the setting of the switches in the **pin** electronic circuits together with the electrical manifestation (logical

one, or logical zero) impressed on the input of the **pin** electronic circuits, dictates the electrical characteristics and magnitude of the electrical manifestations impressed on the associated **pins** of the device under test.

SUMM In summary, in response to the application of each of said n binary bit words on said n **pin** electronics circuits, and under control of said operational test program, each of said n **pins** of the device under test will be subjected to an electrical manifestation or the absence of an electrical manifestation in accordance with its function. For example, the logical input **pins** will receive an

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electrical manifestation of a logical one or an electrical manifestation of a logical zero as called for by the test program, the power supply **pins** will receive a voltage forcing or current forcing electrical manifestation as called for by the test program, the load **pins** will be subjected to an appropriate electrical load as called for by the test program, the output **pins** will be conditioned to receive an output from the device under test as directed by the test program, etc.

SUMM The tester further contains circuitry, which may be in the n **pin** electronic circuits and/or system controller for accepting, in response to each of said n-binary bit words, an output from the output **pins** of the device under test and comparing it with a known standard.

SUMM . . . time developing very rapidly. Merely by way of example, it will be apparent that the technique employed to set-up the **pin** circuits may take any one of many forms. For example, it may be accomplished more or less exclusively by decode. . . by the system controller jointly with decode type circuitry, or by the system controller directly and alone. Further the n **pin** circuits need not be identical. Certain of said **pin** circuits may be capable of performing functions that others of said **pin** circuits are not capable of performing. As will be seen and appreciated more fully from the hereinafter detailed description of. . . practice of applicant's invention is not limited to a particular tester structure, nor to a particular technique of conditioning the **pin** circuits, or comparing the output of the device under test with a known standard and storing, manifesting, and/or analyzing the. . .

SUMM . . . mix of serial and parallel data. For example, parameter and set-up data is applied to all Device Under Test (DUT) **Pins** in parallel. Primary DUT I/O **pins** feeding combinatorial and random sequential logic also require parallel application of test data. However when shift register structure, counter structure,. . . characteristics exist in the device or structure under test, long serial chains of data must be applied to a single **pin**, or a limited number of **pins**, between applications of parallel data. This is what will be referred to as Mixed-Serial-Parallel (MSP) Testing. Mixed-Serial-Parallel test patterns are. . .

SUMM . . . The shift register then conveys, in parallel, said one of said n words to latch means contained within the n **pin** circuits. Thereafter the shift register accepts the word, x, in parallel and provides a serial by bit output at a register position corresponding to the said binary bit position, y, of said n words. The **pin** circuit of said binary bit position y successively accepts said serial by bit output. The parallel to serial conversion of. . .

SUMM A still further object of the invention is to provide an improved **pin** circuit for use in a high speed electronic tester.

SUMM A still further object of the invention is an improved **pin** circuit for use in a high speed electronic tester employing binary word reconstruction means.

DRWD FIG. 6 discloses a logical block diagram of the **pin** circuit employed in the preferred embodiment;

DRWD . . . block diagram of the hazard free polarity hold latch employed in the Shift Register means of FIG. 4 and the **Pin** Circuit of FIG. 6;

DETD . . . a block diagram schematically representing the data flow in a typical prior art tester for testing a device having n **pins**, P1 through PN. The n **pin** electronic circuits PE1 through PEN

are respectively associated with **pins** P1 through PN. Each **pin** electronic circuit includes the digital to analog circuits for driving the device under test, analog to digital circuits for detecting the device under test outputs and registers for holding the status of each of the **pins**. Each of the **pin** electronic circuits includes switches controlled by signals on leads 5. The switches activate circuits within the **pin** electronics circuit in accordance with the function to be performed thereby, such as driver, detector load, power supply, ground and open circuit. It will be appreciated that during any perticular test step certain **pin** electronic circuits will be performing a driver function, while others of said **pin** electronic circuits will be performing an output functi

function, while still others of said **pin** electronic circuits may respectively be performing the functions load, power supply, ground and/or open circuit.

DETD . . . appropriate signals on leads 5 for controlling and designating the function of each of said, PE 1 through PE n **pin** electronic circuits. The n bits of each word provide each of the PE 1 through PE n **pin** electronic circuits with a logical one, or logical zero, electrical manifestation as called for by a test pattern, under control.

. .

DETD . . . Controller and Bulk Store 1 provide signals on leads 5. The signals on leads 5 instruct and specify to each **pin** electronic circuit what function it is to perform.

DETD . . . in a different manner the four bits contained within bit positions, ba, bb, bc, bd are decoded and tell the **Pin** Electronic Circuits how to interpret the n bits contained within bit positions b1, b2 through bn. The four bits provide. . .

DETD a. test normally; (b) set up input **pins** c. set up output **pins**; (d) mask outputs e. change I/0-----etc.-----through sixteen operational codes.

DETD Set up **Pin** Electronic circuits. Namely set the appropriate **pin** electronic registers for each of the **pins** that are to be employed as inputs; set the appropriate **pin** electronic registers for each of the **pins** that are to be employed as outputs; and so on as to the remaining **pin** circuits and their respective functions. Note: During each test step where test data is applied to the **pin** circuits, each **pin** circuit associated with a **pin** of the device under test will be in the condition required to perform its function. This conditioning will have taken. . . in time to application of test data in the form of electrical manifestations of logical ones and zeros to the **pin** circuits. It will be appreciated that certain **pin** electronic circuits may not have a function to perform during one or more test steps. These non-performing **pin** electronic-circuits will have been appropriately conditioned, or de-conditioned. The **pin** circuits having been set up to perform their respective functions, each of said **pin** circuits will simultaneously have impressed thereon an electrical manifestation of either a logical one or a logical zero as dictated by the test pattern step. The output of the device under test will be received by certain of the **pin** electronic circuits. This output will be compared to a known standard, or Expected Result. The output from each output **pin** of the device under test will be compared with an expected good output from that output **pin** under the conditions of the particular test step. This comparison may take place in the **pin** electronics circuits and the result (Pass/Fail) electrically manifested and conveyed to the System Controller and Bulk Store 1, over cable leads 5 and 6. Thus it is apparent that the Pass/Fail data for each output **pin** of the device under test, for each test step is available for storage, processing and/or analysis by the System Controller. . . each subsequent test step a successive one of said m binary words is impressed on the inputs of said n **pin** circuits and the operational code specifying inputs of said Decode circuit. Assume for convenience of explanation that the subsequent test. . . subsequent test steps a successive one of said m binary words will be impressed on the inputs of said n **pin** circuits and said inputs of the Decode Circuit. Further assume for purposes of explanation that the

operation code specifying bits. . . calls for "Test Normal, " and thereby no change, or modification, in the respective functions of each of the n **pin** circuits is called for. The word oriented Random Access Memory 2 will successively apply, one during each test step, a. . . one of said m words on said aforeidentified input terminals. During each said test steps Pass/Fail data for each ouput **pin** of the device under test is made available for storage, processing and/or analysis by the System Controller 1. It will. . .

DETD . . . interconnected components and contains a shift register type structure requiring a periodic input of logical ones and zeros on input **pin** Pn-70 during test steps 1 through P-7, where P is the integer one hundred seven. Further assume n is equal. . . and that during said 1 through P-7 test steps the logical ones and zeros respectively impressed on said n input **pins**, with the exception of input **pin** n-70, are invariant. It will be apparent that one hundred of said p words are identical, except for bit position. . .

DETD . . . modification includes the provision of word reconstruction means coupling a memory, such as word oriented Random Access Memory, to the **pin** circuits of the tester. The use of word reconstruction means has, as one primary advantage the material reduction of the. . .

DETD . . . the tester to assume the "set-up mode " or the "test mode." In the set-up mode, each of said n **pin** circuits receiving a logic one from the RAM is set to the status indicated by the operational code.

The **pin** circuits receiving a logic zero do not change. Correspondingly the architecture of the tester may be such that the operational code Mask Outputs is executed in the test mode whereby the output from predetermined ones of the output **pins** of said devices under test are masked. The masking of an output from a **pin**, as desired, results in the ignoring of the output of that particular output **pin**.

DETD . . . said m words contains bit positions b1, b2, b3----b(n--2), b(n--1), bn and b01, b02---b0(x-1), box. In this illustrative example the **pin** circuits PE-1 through PE-N have already been set-up, namely each **pin** circuit has been conditioned to perform its required function. The operational code specifying bits for each of said m words. . .

DETD During each successive test steps, a successive one of said test words, m.sub.1 through m.sub.m, is applied to the **pin** circuits and decode circuit 4. Namely, test word m.sub.1 is applied during test step 1. Test word m.sub.2 is applied. . .

DETD Still referring to FIG. 2 and specifically test words m.sub.1 through m.sub.100, it will be seen that **pin** circuits PE1 through PEN each receive test data, namely an electrical manifestation of either a logical one or a logical. . . and 101, respectively, as called for by the test pattern, and that during test steps 2 through 100, respectively, only **pin** circuit PE3 receives an electrical manifestation of a logical one or logical zero as called for by the test pattern.. . .

DETD Thus in the example illustrated in FIG. 2 **pin** circuit PE3 receives a serial test data string ninety-nine data bits long (test steps 2 through 100) between the parallel data tests (test steps 1 and 101) in which each of said n **pin** circuits PE1 through PEN receives a data bit. This condition is represented in FIG. 2 by bit positions b1 through. . .

DETD . . . cable leads 6. Decode circuitry 4 is coupled to closed loop Shift Register 100 by cable leads 3 and to **Pin** Electronic circuits PE 1 through PE N by cable leads 5. Shift Register 100 is coupled between the output of RAM 2 and the inputs of **pin** circuits PE 1 through PE N.

DETD . . . to receive an input from a bit position of RAM 2 and provides an output to the input of a **pin** electronic circuit. From FIG. 3 it will be seen that: bit position s.sub.1 of register 100 is coupled between bit position b.sub.1 of RAM 2, and via lead s.sub.1 to **pin** circuit PE 1; bit position s.sub.2 of register 100 is coupled between bit position b.sub.2 of RAM 2, and via lead s'.sub.2 to **pin** circuit PE 2; --- ---- -- -----; bit position s.sub.(n-1) of register 100 is coupled between bit position b.sub.(n-1) of RAM 2, and via lead s'.sub.(n-1) to **pin** circuit PE-(n-1); and bit position s.sub.n of register 100 is coupled between bit position b.sub.n of RAM 2 and via lead s'.sub.n to **pin** circuit PE-N. Shift Register 100 has a closed loop, or connection 100C between register stage (bit position) s.sub.1 and register. . . . an n-bit binary word, in parallel, from RAM 2 and, in parallel, impress said n bit binary word on the **pin** circuits PE-1 through PE-N. Shift Register 100 is still further controllable to accept an n-bit binary word in parallel from. . .

DETD Referring to FIG. 3, assume for convenience of explanation that **Pin** circuits PE-1 through PE-N have each been set up to perform their respective functions. Then during the next subsequent test. . . . as a large gate permitting test word m.sub.1 to pass in parallel through Shift Register 100 and be applied to **pin** circuits PE-1 through PE-N. The remaining portion of this test step has been discussed earlier herein.

DETD It is however to be appreciated that each **pin** circuit functioning as other than an output, will maintain the condition arrived as a result of an input from a preceding test word, until it is conditioned to receive a subsequent input. Thus the **Pin** circuits conditioned to function as inputs, energy sources, opens, or grounds will maintain the electrical state arrived at as a. . .

DETD . . . as a gate and impress the binary bit value from bit position b.sub.3 of said word on the input of **pin** circuit PE-3.

DETD . . . is a matter of design choice as to how this is accomplished. It will also be appreciated that when only **pin** circuit PE-3 is to receive an input, it is matter of design choice whether only stage s.sub.3 of register 100 is conditioned to provide an output, or whether only **pin** circuit PE-3 is conditioned to receive an input.

DETD In the above discussed test step only **pin** circuit PE-3 received an input. Except for **pin** circuits functioning as an output from the device under test, all **pin** circuits maintained their status which was arrived at in response to test word m.sub.1. Since test word m.sub.1 and m.sub.2 differ only, if at all, in bit position b.sub.3 the impressing of a single input on **pin** circuit PE-3 has effectively executed the test step called for by test word m.sub.2.

DETD . . . stage s.sub.3 to function as a gate during each of these test steps. Whereby during each of these test steps **pin** circuit PE-3 is the only one of said n **pin** circuits which will receive an input.

DETD . . . Steps 2 Through 101

Test Step No.	Shift Register Stage S.sub.5	Shift Register Stage S.sub.4	Shift Register Stage S.sub.3	Test Data (Binary Bit Value) Impressed on **Pin** Circuit PE 3
2	*3-4	*3-3	*3-2	*3-2

3	*3-5	*3-4	*3-3	*3-3
4	*3-6	*3-5	*3-4	*3-4
5	*3-7	*3-6. . .		

DETD . . . for test steps 2 through 100 in a counter-clockwise direction, as viewed in FIG. 3, it will be seen that **pin** circuit PE-3 receives a binary bit input during each of the test steps 2 through 101.

It will also be recognized from Chart No. 1 that the binary bit input to **pin** circuit PE-3 during test steps 2 through 101, respectively, is the binary bit value of bit position b.sub.3 of test. . . .

DETD . . . activated gate and permits test word m.sub.102 to pass in parallel there through and be applied to the inputs of **pin** circuits PE-1 through PE-N. The completion of this test step, as is conventional for each test step, will include the comparison of the electrical manifestation of each output terminal or output **pin** of the device under test with a known standard. An electrical manifestation indicative of the merit or lack of merit. . . .

DETD . . . through m.sub.202. In this illustrative example bit position b.sub.3 of the test word corresponding to shift register stage s.sub.3 and **pin** electronic circuit PE-3 has been again selected for convenience of illustration. It will be appreciated that the bit location in. . . .

DETD . . . FIG. 3 and in the preferred embodiment a clock pulse source provides at least one clock pulse to any DUT **pin** or **pins** (except the test serial data **pin**) during Test Serial operation. It is within the skilled of the art to provide an additional clock source, or sources,. . . .

DETD . . . conditioned to impress the binary bit value contained within bit position b.sub.3 of the afore-identified word on the input of **pin** circuit PE-3.

DETD In test steps 103 through 202 only **pin** circuit PE-3 and the Clock 1 **pin**, or **pins**, receive inputs during each of said steps. All other **pin** circuits, with the exception of **pin** circuits functioning as outputs, maintain through latch or storage structure contained therein, their respective electrical state or condition arrived at in response to an input from test word m.sub.102 during test step 102. The **pin** circuits performing an output function are respectively conditioned to accept an output from the device under test during each test. . . .

DETD It is to be appreciated that if the Test Serial **pin** (in the example **pin** P-3 and **pin** circuit PE-3) had been set-up as an output, then the serial test data would be used as the expected DUT. . . . Go/No Go signal developed for each test step. As with inputs, Clock 1 (CL1) would be activated and all other **pin** circuits would remain constant.

DETD . . . Steps 103 through 202

Test Step No.	Shift Register Stage S.sub.5	Shift Register Stage S.sub.4	Shift Register Stage S.sub.3	Test Data (Binary Bit Value) Impressed on **Pin** Circuit PE-3
103	*3-105	*3-104	*3-103	*3-103
104	*3-106	*3-105	*3-104	*3-104
105	*3-107	*3-106	*3-105	*3-105
106	*3-108	*3-107	*3-106. . .	

DETD . . . per test step in a counter clockwise direction as viewed in FIG. 3 during test steps 102 through 201. Only **pin** circuit PE-3 receives an input, namely a binary bit value of logical one or logical zero during each of the test steps 103 through 202. The binary bit value of test data that **pin** circuit PE-3 receives during

each of the test steps 103 through 202 is respectively the binary bit value of bit. . .

DETD In the prior example of the operation of the tester of FIG. 3 only a single **pin** circuit (PE-3) received a serial input of binary test data. It will be apparent that the structure of FIG. 3 is capable of supplying a serial input of binary test data to more than one of said n **pin** circuits during a test step. For example, assume two **pin** circuits respectively coupled to two adjacent stages of the shift register require a serial input of test data. By causing. . . two stages per test step and appropriately gating the content of the two adjacent shift register stages to the two **pin** circuits this can be accomplished. The same approach can be taken to provide serial binary test data to three or more **pin** circuits respectively connected to three or more adjacent stages of the shift register. In this situation the shift register would. . .

DETD It will also be apparent that two or more **pin** circuits respectively connected to non-adjacent stages of the shift register may each be provided with a serial of input of. . .

DETD . . . register structure and appropriate controls may be appropriately coupled in more or less parallel fashion between the RAM and the **pin** circuits. Each of these two registers will be independently controlled and respectively provide serial/parallel test data to a **pin** circuit, or **pin** circuits.

DETD . . . an entire test pattern for a given part number. Conventional RAM's have a capacity of 1,000 to 4,000 bits per **pin** and may by the practice of applicant's invention contain the entire test pattern for a given part number.

DETD Faster test speed due to using high speed shift register and **pin** circuits. Normally the RAM's are practically limited to 50 to 200 nsec cycle time making test rates equal to or greater than 5 to 20 MHZ. The **pin** circuits and shift register circuits total only a few circuits and are much faster. When 20 nsec circuits are employed in the **pin** circuits and shift register there is an additional multiple of up to ten improvement in the testing speed.

DETD Only a limited amount of additioanl hardward is required. Namely one shift register stage per **pin** circuit and limited additional control and decode logic structure.

DETD . . . stored in and executed from a solid state RAM with as many parallel outputs as there are devices under test **pins**. Furthermore, complex LSI logic requires many changes of **pins** from Input to Output, Masked to Not-Masked (i.e., of No-Go information), and Load to No-Load on any **pin** or **pins** mixed in with the I/O test sequences. The preferred embodiment in addition to the earlier enumerated advantages obtained by practicing. . .

DETD . . . as, "Drive Time," "Strobe Time," "X-Time," "Y-Time," and "Clock 1" time. The System Controller also provides Analog levels to the **pin** circuits coupled to the output **pins** of the device under test. The results from the comparison of the output from the device under test and the. . .

DETD Stated differently the System Controller generates and provides appropriate analog levels and limits used in the **Pin** Electronic circuits and receives Go/No Go data from the **Pin** Electronic circuits.

DETD . . . the RAM and provides electrical manifestations, calling for the specified operation, to the Shift Register Means (FIG. 4) and the **Pin** Electronic Circuits (FIG. 6). The information conveyed from the Decode circuitry to the **Pin** Electronic circuits and the Shift Register Means is bussed in parallel. The **Pin** electronic circuits receive per-**pin** or per-**pins** information

fromthe Shift Register and the RAM via leads S'.sub.1 through S'.sub.n, respectively.

DETD . . . 89, 90, 91 and 97, and via the lead designated T, for Test Mode, is conveyed to each of the **PIN** Electronic Circuits. The output of AND circuit 86 is UP for the logical condition abcdy and conveys to each stage. . . Y-Time. The output of AND circuit 87 is UP for the logical condition abody and conveys to each of the **PIN** Electronic Circuits the instruction, or operational code, SD (Set Disconnect) at Y-Time. The output of AND circuit 88 is UP for the logical condition abcdy and conveys to each of the **PIN** Electronic Circuits the instruction SPS (Set **PIN** Serial) at Y-Time. The output of AND circuit 89 is UP for the logical condition abcd and conveys to each of the **PIN** Electronic Circuits the instruction TP (Test Parallel. The output of AND circuit 91 is UP for the logical condition abcd and conveys to each of the **PIN** Electronic Circuits the instruction TT (Test Tester). The output of AND circuit 92 is UP for the logical condition ay and via the lead designated SU, the **PIN** circuits are informed at Y-Time that the tester is in the SET-UP Mode of operation.

DETD The output of AND circuit 90 is UP for the logical condition abcd and conveys to each of the **PIN** Electronic Circuits the instruction TS (Test Serial). The output of AND circuit 90 is also connected to the input of. . .

DETD . . . 84 at Y-time The output of AND circuit 98 is designated as SC1 (SET CLOCK 1) and conveyed to each **PIN** Electronic Circuit.

DETD . . . Latch of FIG. 7 is a hazard free latch employed in the Shift Register Means of FIG. 4 and the **PIN** circuit of FIG. 6.

DETD . . . of the Shift Register Means stores the test data obtained from the RAM and impresses the test data on the **pin** electronic circuits. The NST portions of the Shift Register Means, as explained hereinafter, controls the number of serial tests to. . .

DETD . . . of Latch 51 is also impressed on the data inputs D of Latches 52 and 53 and is conveyed to **Pin** Circuit PE3. Now further assume that during the test step m-100 an operational code other than SNST (Set number of. . . shift register has been completed, namely the storing of test data and the conveying of the test data to the **Pin** Circuits. The operational codes and the logical requirements calling for a particular operation, as set forth in FIG. 10, will. . .

DETD . . . (1111) namely Test Parallel (TP). AND circuit 89 of the Decoder (FIG. 8) will be energized and appropriately condition the **PIN** Electronic circuits as explained hereinafter. Also, since AND circuit 90 of the Decoder is not energized the TS inputs of. . . UP or DOWN state of each Latch 51 is impressed via leads S.sub.1 through S.sub.n respectively on the inputs of **PIN** Electronic Circuits PE1 through PEN.

DETD . . . of discussion that the predetermined bit position is b.sub.3 of the test word. Namely the bit to be impressed on **PIN** Electronic circuit PE-3 during the test steps M-121 through M-22. Also accept at this time, subject to complete detailed explanation hereinafter, that the **PIN** Electronic circuits have throughout these examples been appropriately set-up.

DETD . . . test word, consisting of logical ones and zeros; Latch 53 of stages S.sub.n contains therein a logical "one"; and only **PIN** Electronic Circuit PE3 is conditioned to receive a test data input. All **PIN** circuits other than PE-3 are precluded from accepting a test data input. For test-step M-121 the operational code changes to. . .

DETD . . . or read out, express provision is made in the preferred embodiment for applying a clock, (Clock 1) to any DUT **pin**, or **pins**, requiring the same. Additional clocks may be provided as

needed in a similar manner.

DETD The Operational Code SET CLOCK 1 (SCl) is called for by the Operational Code specifying bits abcd (1011). Any **PIN** Electronic Circuits receiving a logical one during the execution of a SET CLOCK 1 operation will have its Latch 35. . . 35 (FIG. 6)] Referring to FIG. 6 and specifically Latch 35 and AND circuit 36 it will be seen that **Pin** circuits having a logical one stored in Latch 35 will accept Clock 1 pulses during a TEST SERIAL Operation. Referring. . .

DETD . . . test cycle, or test step, (in this example test steps 121 through 22) of the TEST SERIAL Operation the pre-conditioned **PIN** Electronic Circuit, or Circuits, will receive a Clock 1 (CL1) pulse.

DETD . . . portion of stage S.sub.1 signals the completion of the Serial Test Operation; during a Serial Test Operation only any one **PIN** Electronic circuit is conditioned to accept a test data input. (PE 3 in the above example).

DETD . . . (b.sub.1), Data In (b.sub.2), Data In(b.sub.3)--- --- Data In (b.sub.n-1), and Data In (b.sub.n) and provides test data to the **PIN** Electric circuits PE1 through PEN via leads S.sub.1 ' through S.sub.n '. As explained earlier herein, during a Test Serial.

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DETD **Pin** Electronic Circuit (FIG. 6)

DETD FIG. 6 discloses the logical circuit diagram of one of n like **PIN** Electronic circuits. Test data from each stage of the Shift Register Means is impressed on the input of the **PIN** Electronic circuit connected thereto.

DETD The operation of the **PIN** Electronic circuits will be undertaken by utilizing a number of operational codes. There are n **PIN** circuits. One for each stage of the Shift Register Means.

DETD . . . FIG. 6 will be conditioned by a y-time pulse, when a logical one of test data is impressed on the **PIN** circuit input. Thus at y-time the clock input of each of the polarity latches 22, 23 and 24 will be. . . input thereto at y-time. Namely, the output of Latch 22 will be UP, where the test data input to the **PIN** circuit is a logical one, for the following operational codes:

DETD . . . switches 32 and applies the load, represented as a resistor connected between switch 32 and potential source V.sub.4, to the **pin** of the device under test. As schematically represented in FIG. 6, the load is applied via switch 32 connection J.sub.1 and switch 34 to the **pin** of the device under test.

DETD The Operational code 0100, SET-LOAD, OUT, MASK, (SLIM) as recited above,
applies a load to the **pin** of the device under test.

DETD The Operational code 0101, SET-LOAD, OUT, MASK, (SLIM) as recited above,
applies a load to the **pin** of the device under test. Also, the presence of the d bit of the operational code specifying bits causes the. . .

DETD The Operational code 0110, SET-LOAD, IN, MASK, (SLIM) as recited above, applies a load to the **pin** of the device under test. Also, the presence of the c bit of the operational code specifying bits causes the. . . 29, as schematically represented, through switches 33 and
32
to the load and through switches 33 and 34 to the **pin** of the device under test. Thus the Operational code SLIM connects the Driver
29
to the DUT **pin**, applies the Load to the DUT **pin**, and unmasks the rendition of the GO/NO GO manifestation.

DETD The Operational code 0111, SET-LOAD, IN MASK (SLIM), as recited above, applies a load to **pin** of the device under Test (DUT). Also, the presence of the c and d bits of the Operational code specifying. . . 29, as schematically represented, through switches 33 and 32 to the load, and through switches 33 and 34 to the **pin** of the device under test. Thus the operational code SLIM connects the Driver 29 to
the